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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/786,049	06/18/2001	Mitsuru Sato	1086.1141	6861

21171 7590 11/14/2003

STAAS & HALSEY LLP
SUITE 700
1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
PATEL, HETUL B	

ART UNIT	PAPER NUMBER
2186	8

DATE MAILED: 11/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/786,049	SATO ET AL.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 June 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3*
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. Claims 1-16 are presented for examination.

2. A substitute specification in proper idiomatic English and in compliance with 37 CFR 1.52(a) and (b) is required. The substitute specification filed must be accompanied by a statement that it contains no new matter.

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

4. Claim 6 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. In this application, the claim 6 has the same content as to that of the claim 3.

5. Applicant is advised that should claim 10 be found allowable, claim 11 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 7 and 16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Both in the specification and claims 7 and 16 of this application, it states that "when none of the other cache devices store the corresponding data, the pre-fetch data is invalidated; and when the other cache devices share the corresponding data, the pre-fetch data is stored as it is". It is not understood that if the other cache devices do not contain the data corresponding to the pre-fetch data, then why the pre-fetch data get invalidated?

Claims 8 and 9 are also rejected since they are dependent upon the indicated rejected claim 7.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 7, 12 and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claims are generally narrative and indefinite, failing to conform with current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors.

The limitation "the other cache device" recites in lines 9, 12 and 13 of the claim 7 and in lines 21 and 23 of the claim 16. There is insufficient antecedent basis for this limitation in the claim.

Claim 12 recites the limitation "said interconnecting network" in line 3, "the preservation states" in line 6 and "the state controlling lines" in line 7. There is insufficient antecedent basis for this limitation in the claim. Also, Lines 6-16 of the claim 12 are not clear and need to be updated appropriately.

Claims 7 and 16 also contains many other grammatical deficiencies, for example, a comma "," is required in the line 7 of the claim 7 after the word "processors" and in the line 10 of the claim 7, after the word "memory". Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-5, 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Naruse et al. (USPN: 6,526,480), hereinafter, Naruse.

With regards to claim 1, Naruse teaches a cache device setup (e.g. 10-1, 10-2, ..., 10-n in Fig. 6) in each of processors(e.g. 12-1, 12-2, ..., 12-n in Fig. 6), interconnected to other cache devices in other processors and connected to main memory (e.g. 16 Fig. 6), which comprises:

- a cache memory in which a part of the data in the main memory is stored in one or more cache lines and a state tag using to manage data consistency is set up in each of the cache lines (e.g. see Col. 1, lines 26-29 and Col. 4, lines 17-23), and
- a cache controller for carrying out a weak read operation for causing failure in said pre-fetch request as fetch protocol (e.g. see Col. 4, lines 27-60).

However, Naruse does not teach that the cache controller for carrying out a weak read operation for causing failure in said pre-fetch request as fetch protocol, in the case that at the time of the generation of a pre-fetch request following a read request from one of the processors, the data stored in the other cache devices cannot be read unless its state tag is changed. But it is very well known that in any computer system with the cache memory, when a cache miss occurs, the cache memory fetches/accesses the data requested by the processor from the main memory and at the same time it also pre-fetches the data, i.e. it also fetches the data, which most likely to be called by the processor in future, and stores this data in the cache. Thus, pre-fetch following a read request always occurs in these systems, in order to improve the system performance by reducing the number of cache misses. In the MESI protocol, which is very well

known in the art, whenever the data stored in other cache devices is in the exclusive state, this data cannot be read by the current cache device unless the state tag of the data stored in other cache devices get changed and thus the pre-fetch request, which need to read the data from the other cache devices cannot run successfully unless the state tag of the data stored in the other cache devices get changed and thus the pre-fetch request get failed, in order to maintain the data consistency in the system.

With regards to claim 2, Naruse discloses the claimed invention as described above and furthermore teaches that the cache memory distinguishes the stored data by a data-modified state (M), an exclusive state (E), a data-shared state (S) and an invalid state (I), each of which indicates validity of the state tag (e.g. see Col. 1, line 61 to Col. 2, line 35 and Fig. 2A-2B). When the data requested by the pre-fetch request is stored in the other cache devices in either the data-modified state (M) or the exclusive state (E), most likely the pre-fetched data is not the most updated data since the data might be changed which is stored in either the data-modified state (M) or the exclusive state (E) in other cache devices. Therefore the pre-fetch request has to fail in order to maintain the data consistency throughout the cache device.

With regards to claim 3, Naruse discloses the claimed invention as described above. However, Naruse does not teach that the cache controller reads the data from the main memory if the data corresponding to the pre-fetch request is stored in other cache devices in the invalid state and it reads the data from the other cache devices if the data corresponding to the pre-fetch request is

stored in other cache devices in the shared state. In the MESI protocol, which is well known in the art, if the data corresponding to the pre-fetch request is stored in the other cache device in the invalid state, it reads the valid data, which is stored in the main memory and stores it in the exclusive state and if the data corresponding to the pre-fetch request is stored in the other cache device in the shared state, it reads the data from one of those devices since data in those devices is most up-to-date and valid data compare to the main memory data and stores it in the shared state until it modified by that or other cache device to maintain the data consistency.

With regards to claim 4, Naruse teaches a cache device setup (e.g. 10-1, 10-2, ..., 10-n in Fig. 6) in each of processors (e.g. 12-1, 12-2, ..., 12-n in Fig. 6), interconnected to other cache devices in other processors and connected to main memory (e.g. 16 Fig. 6), which comprises:

- a cache memory in which a part of the data in the main memory is stored in one or more cache lines and a state tag using to manage data consistency is set up in each of the cache lines (e.g. see Col. 1, lines 26-29 and Col. 4, lines 17-23), and
- a cache controller for carrying out a pre-fetch protocol that in the case that at the time of the generation of a pre-fetch request following a read request from one of the processors, the data stored in the other cache devices cannot be read without changing its state tag, the data is read without changing the state tag and stored in the cache memory with the setup of a weak state W, and at the time of synchronization

operation, to attain data-consistency by software the data in the cache memory in weak state (W) is wholly invalidated by the "weak invalidating operation"(e.g. see Col. 4, lines 27-60).

In any computer system with the cache memory, when a cache miss occurs, the cache memory fetches/accesses the data requested by the processor from the main memory and at the same time it also pre-fetches the data, i.e. it also fetches the data, which most likely to be called by the processor in future, and stores this data in the cache. Thus, pre-fetch following a read request always occurs in these systems, in order to improve the system performance by reducing the number of cache misses. In the MESI protocol, which is very well known in the art, whenever the data stored in other cache devices is in the exclusive state, this data cannot be read by the current cache device unless the state tag of the data stored in other cache devices get changed and thus the pre-fetch request, which need to read the data from the other cache devices cannot run successfully unless the state tag of the data stored in the other cache devices get changed and thus the pre-fetch request get failed, in order to maintain the data consistency in the system.

With regards to claim 5, Naruse discloses the claimed invention as described above and furthermore teaches that the cache memory distinguishes the stored data by a data-modified state (M), an exclusive state (E), a data-shared state (S) and an invalid state (I), each of which indicates validity of the state tag (e.g. see Col. 1, line 61 to Col. 2, line 35 and Fig. 2A-2B). When the data requested by the pre-fetch request is stored in the other cache devices in

either the data-modified state (M) or the exclusive state (E), most likely the pre-fetched data is not the most updated data since the data might be changed which is stored in either the data-modified state (M) or the exclusive state (E) in other cache devices. Since the validity of that particular data is not known, the cache controller stores that data in the cache memory with the setup of the weak state (W), and at the synchronization operation, the cache controller changes the validity of that data from weak state (W) to invalid state (I) wholly to maintain the data consistency throughout the cache device (e.g. see Col. 4, lines 27-60).

With regards to claim 12, the examiner interpreted the claim as following: "The cache device according to claim 11, wherein said interconnecting network is a snoop bus". Naruse discloses the claimed invention as described above and furthermore teaches that the cache apparatuses 10-1 to 10-n are mutually connected by a system bus 14 and further connected to a main storage 16 by the system bus 14. For example, a snoop bus is used as a system bus 14 for connecting the cache apparatuses 10-1 to 10-n (e.g. see Col. 11, lines 20-24 and Fig. 6).

With regards to claim 14, Naruse teaches a method for controlling a cache system wherein cache devices setup (e.g. 10-1, 10-2, ..., 10-n in Fig. 6) in respective processors (e.g. 12-1, 12-2, ..., 12-n in Fig. 6) are mutually connected through an interconnecting network (e.g. see 14 in Fig. 6)and are connected to a main memory (e.g. see 16 in Fig 6), which comprises the steps of:

- storing a part of the data in the main memory in one or more cache lines on cache memory and setting up a state tag using to manage the

data consistency in each of the cache lines (e.g. see Col. 1, lines 26-29 and Col. 4, lines 17-23), and

- carrying out a weak read operation for causing a failure in the pre-fetch request as a fetch protocol (e.g. see Col. 4, lines 27-60).

However, Naruse does not teach that the cache controller for carrying out a weak read operation for causing failure in said pre-fetch request as fetch protocol, in the case that at the time of the generation of a pre-fetch request following a read request from one of the processors, the data stored in the other cache devices cannot be read unless its state tag is changed. But it is very well known that in any computer system with the cache memory, when a cache miss occurs, the cache memory fetches/accesses the data requested by the processor from the main memory and at the same time it also pre-fetches the data, i.e. it also fetches the data, which most likely to be called by the processor in future, and stores this data in the cache. Thus, pre-fetch following a read request always occurs in these systems, in order to improve the system performance by reducing the number of cache misses. In the MESI protocol, which is very well known in the art, whenever the data stored in other cache devices is in the exclusive state, this data cannot be read by the current cache device unless the state tag of the data stored in other cache devices get changed and thus the pre-fetch request, which need to read the data from the other cache devices cannot run successfully unless the state tag of the data stored in the other cache devices get changed and thus the pre-fetch request get failed, in order to maintain the data consistency in the system.

With regards to claim 15, Naruse teaches a method for controlling a cache system wherein cache devices setup (e.g. 10-1, 10-2, ..., 10-n in Fig. 6) in respective processors (e.g. 12-1, 12-2, ..., 12-n in Fig. 6) are mutually connected through an interconnecting network (e.g. see 14 in Fig. 6)and are connected to a main memory (e.g. see 16 in Fig 6), which comprises the steps of:

- storing a part of the data in the main memory in one or more cache lines on cache memory and setting up a state tag using to manage the data consistency in each of the cache lines (e.g. see Col. 1, lines 26-29 and Col. 4, lines 17-23),
- setting up the weak state (W) to the data whose validity is unknown, i.e. the data which got read without changing the state tag to respond to the processor, and wholly invalidating the data in the cache memory in the said weak state (W) at the time of synchronization operation of memory consistency by software (e.g. see Col. 4, lines 27-60).

In any computer system with the cache memory, when a cache miss occurs, the cache memory fetches/accesses the data requested by the processor from the main memory and at the same time it also pre-fetches the data, i.e. it also fetches the data, which most likely to be called by the processor in future, and stores this data in the cache. Thus, pre-fetch following a read request always occurs in these systems, in order to improve the system performance by reducing the number of cache misses. In the MESI protocol, which is very well known in the art, whenever the data stored in other cache devices is in the exclusive state, this data cannot be read by the current cache device unless the

state tag of the data stored in other cache devices get changed and thus the pre-fetch request, which need to read the data from the other cache devices cannot run successfully unless the state tag of the data stored in the other cache devices get changed and thus the pre-fetch request get failed, in order to maintain the data consistency in the system.

9. Claims 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Naruse in view of Gornish et al. (USPN: 5,752,037), hereinafter, Gornish.

With regards to claims 10-11, Naruse discloses the claimed invention as described above. Naruse does not teach that when processor sends a read request to the cache controller, the cache controller carries out a pre-fetch request for pre-fetching data in one or more addresses adjacent to a read-requested address after the read request. However, Gornish teaches that when a cache miss occurs, the cache memory device fetches the data requested by the processor from the main memory and at the same time it also pre-fetches the data, i.e. it also fetches the data, which most likely to be called by the processor (i.e. data in one or more addresses adjacent to a read-requested address) in future, and stores this data in the cache (e.g. see Col. 1, lines 25-35 and Col. 2, lines 11-20). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the Naruse's cache device by adding an extra function to the cache controller so it can carry out a pre-fetch request for pre-fetching data in one or more addresses adjacent to a read-requested address after the read request as taught by Gornish to reduce the number of cache misses because most of the times the next read

request sent by the processor is the address adjacent to currently read memory address.

10. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Naruse in view of Steely, Jr. et al. (USPN: 5,966,737), hereinafter, Steely.

With regards to claim 13, although Naruse discloses the claimed invention as described above, Naruse does not teach that in the case when the simultaneous requests of read and pre-fetch requests arises, the data making the distinguishing bit valid are transmitted. However, Steely discloses that the bit ram is used to provide a bit number of any bit, which differs between the tags at the same location in the different banks (e.g. see abstract). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the Naruse's cache device by adding the distinguishing bit as taught by Steely to distinguish the data in the case when the simultaneous read and pre-fetch requests occurs and sending the data which makes the distinguishing bit valid. By using the distinguishing bit, sending data requested by the read request to the processor as a response of the pre-fetch request and vice versa can be avoided.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is (703) 305-6219. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

HBP

TUAN V. THAI
PRIMARY EXAMINER